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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,374	11/13/2003	Rajen Chanchani	SD7151/S98758	1623

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,374	CHANCHANI, RAJEN	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/713374 Attorney's Docket #:SD7151/S98758
Filing Date: 11/13/12003;

Applicant: Chanchani

Examiner: Alexander Williams

Applicant's Amendment filed 2/6/06 to the election of Group I (claims 1 to 12), filed 9/27/05, has been acknowledged.

This application contains claims 13 to 16 drawn to an invention non-elected without traverse.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the further comprising at least one additional stacked layer on the thin chip, each additional stacked layer comprising: a stacked interconnect layer on the top surface of the thin upper chip, the stacked interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the thin upper chip; and a stacked thin chip on the stacked interconnect layer, the stacked thin chip comprising one or more microsystem devices with associated input/output pads on the top surface of the stacked thin chip that are connected to the one or more via capture pads in the stacked interconnect layer by conductive vies through the stacked thin chip in claim 2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 2, 8 to 10 and 12 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, it is unclear and confusing to what is meant by "further comprising **at least one additional stacked layer on the thin chip**, each additional stacked layer comprising: a stacked interconnect layer on the top surface of the thin upper chip, the stacked interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the thin upper chip; and a stacked thin chip on the stacked interconnect layer, the stacked thin chip comprising one or more

microsystem devices with associated input/output pads on the top surface of the stacked thin chip that are connected to the one or more via capture pads in the stacked interconnect layer by conductive vies through the stacked thin chip." Where is this shown in the drawing and detailed in the specification?

In claims 8-10, the phrase "the embedded passive" lack proper antecedent basis. Claim 7 refers to "at least one passive component", but fail to even disclose the claimed "the embedded passive" and the clam leave of –component--.

In claim 12, the phrase " the on or more via" should probably be --the one or more via--.

Any of claims 2, 8 to 10 and 12 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 7, 9, 11 and 12, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Otsuka et al. (U.S. Patent # 6,961,230 B2).

1. Otsuka et al. (figures 1A to 5) specifically figure 5 show a microsystem-on-a-chip, comprising: a bottom chip **22** comprising one or more microsystem devices with associated input/output pads **44,6** on the top surface of the bottom chip; an interconnect layer **(u2,bottom u1)** on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material **1b**, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom chip; and a thin upper chip **(upper u1)** on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to the one or more via capture pads **10** in the interconnect layer by conductive vias **4** through the thin upper chip.

3. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the interconnect layer has a thickness of less than 50 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the compliant dielectric material is a polymer.

6. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the thin upper chip has a thickness of less than 120 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

7. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the interconnect structure further comprises at least one passive component.
9. The microsystem-on-a-chip of Claim 7, Otsuka et al. show wherein the embedded passive comprises a multi-layer capacitor.
11. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the interconnect structure comprises copper.
12. The microsystem-on-a-chip of Claim 1, Otsuka et al. show wherein the on or more via capture pads are sized to control the alignment tolerance of the thin upper chip.

Claims 1, 3, 4 and 6 to 12, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Ho et al. (U.S. Patent # 6,865,089 B2).
1. Ho et al. (figures to 16) specifically figure 12 show a microsystem-on-a-chip, comprising: a bottom chip **31** comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom chip; an interconnect layer **36** on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom chip; and a thin upper chip **42,46** on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to the one or more via capture pads in the interconnect layer by conductive vies through the thin upper chip.

3. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the interconnect layer has a thickness of less than 50 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the compliant dielectric material is a polymer.

6. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the thin upper chip has a thickness of less than 120 microns.
Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

7. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the interconnect structure further comprises at least one passive component.

8. The rnicrosystem-on-a-chip of Claim 7, Ho et al. show wherein the embedded passive comprises a thin film resistor.

9. The microsystem-on-a-chip of Claim 7, Ho et al. show wherein the embedded passive comprises a multi-layer capacitor.

10. The microsystem-on-a-chip of Claim 7, Ho et al. show wherein the embedded passive comprises a spiral inductor.

11. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the interconnect structure comprises copper.

12. The microsystem-on-a-chip of Claim 1, Ho et al. show wherein the on or more via capture pads are sized to control the alignment tolerance of the thin upper chip.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on an interconnect layer and a thin upper chip deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of

obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1, 3 to 7, 9, 11 and 12, insofar as some of them can be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al. (U.S. Patent # 6,889,431 B2).

1. Okabe et al. (figures 1 to 4) specifically figures 1 to3 show a microsystem-on-a-chip, comprising: a bottom chip **23** comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom chip; an interconnect layer **(21, lower portion of 22)** on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material **21** and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom chip; and a thin upper chip **(21, upper portion of 22)** on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to the one or more via capture pads in the interconnect layer by conductive vias through the thin upper chip.

(19) In the manufacturing method of the electronic circuit device using the multi-layered circuit board according to this invention, when the surface of the base substrate is leveled with a resin and the first electrode is disposed thereon, planarity for the first electrode and the thin film dielectric layer to be laminated can be improved. Accordingly, since the thickness of the thin film dielectric layer that can be

laminated without causing defects can be reduced, a thin film capacitor of higher capacitance value can be obtained. As the leveling resin, polyimide or BCB (benzocyclobutene) is practically useful for instance.

(20) Further, the subject of this invention as described above can be solved effectively in an electronic circuit device using a multi-layer circuit board having a thin film capacitor constituted by putting a thin film dielectric layer between a first electrode and a second electrode, by laminating the first electrode layer and the thin film dielectric layer in this order on the base substrate continuously within one identical chamber, then fabricating each of the layers in the order of the thin dielectric layer and the first electrode layer, forming through holes in the base substrate including each of the layers, applying plating to the surface of the base substrate including each of the layers on the side having the first electrode layer and at the inside of the through holes thereby forming a conductor layer constituting the first wiring layer and the second electrode layer to the surface of the base substrate on the side having the first electrode layer and through hole conductors at the inside of in the through holes, and fabricating the conductor layer constituting a first wiring layer and a second electrode layer, thereby forming a conductor pattern of the first wirings connected to the first electrode and a conductor pattern of a second electrode

(21) According to the method as described above, the conductor layer constituting the first wiring layer and the second electrode layer can be formed collectively with the formation of the through hole conductor. Accordingly, the method can simplify the manufacturing steps of the multi-layer circuit board having the thin film capacitor and can reduce the manufacturing.

(22)Then, after fabricating each of the layers in the order of the thin film electric layer and the first electrode layer, when a second connection layer is laminated on the first electrode layer and the thin film dielectric layer and then through holes are formed in the base substrate including each of the layers, the close adhesion strength between the thin film dielectric layer and the conductor layer by plating can be improved by the second connection layer upon fabrication of the conductor layer that constitutes the first wiring layer and the second electrode layer by plating, and contamination for the

surface of the thin film dielectric layer upon forming the through holes can be prevented. Accordingly, this method can improve the production yield and prevent the degradation of the quality of the thin film capacitor.

(24) The foregoing subject of this invention can be solved effectively in an electronic circuit device including a multi-layer circuit board having a thin film capacitor constituted by putting a thin film dielectric layer between a first electrode and a second electrode, by using a metal plate constituting a first wiring layer for the base substrate, laminating a first electrode layer, a thin film dielectric layer, and a second electrode layer in this order on the metal plate continuously within one identical chamber, then fabricating the second electrode layer, thereby forming a conductor pattern including the second electrode, disposing on the second electrode layer an intermediate wiring layer electrically connected through via-holes with the second electrode layer, the first electrode layer or the first wiring layer by way of the dielectric layer and, further, fabricating the first wiring layer and the first electrode layer, thereby forming a conductor pattern including the first electrode.

(5) At first, as shown in FIG. 1A, a leveling resin layer 22 comprising benzocyclobutene of 10 .mu.m thickness is coated by a curtain coat method on a base substrate 21 comprising a polyimide film of 200 .mu.m thickness to level the upper surface of the base substrate. Then, a first electrode layer 11 comprising ruthenium (Ru) of 0.2 .mu.m thickness is laminated by sputtering on the organic polymeric resin layer 22 using a sputtering apparatus (FIG. 1B). Successively, a thin film dielectric layer 20 comprising strontium titanate of 0.3 .mu.m thickness is laminated by sputtering while changing a target in one identical chamber. Strontium titanate is epitaxially grown on the Ru layer by sputtering in an argon atmosphere at an oxygen partial pressure of 10% at a substrate temperature of 250.degree. C. In this invention, it is important that the Ru layer 11 and the thin film dielectric layer 20 thereon are formed in one identical chamber without once opening the chamber. This can form a metal layer on which the dielectric layer can be grown epitaxially and can epitaxially grow the dielectric layer on the metal layer favorably in the state as it is.

3. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the interconnect layer has a thickness of less than 50 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the compliant dielectric material is a polymer.

5. The microsystem-on-a-chip of Claim 4, Okabe et al. show wherein the polymer is benzocyclobutene.

6. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the thin upper chip has a thickness of less than 120 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

7. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the interconnect structure further comprises at least one passive component.

9. The microsystem-on-a-chip of Claim 7, Okabe et al. show wherein the embedded passive comprises a multi-layer capacitor **52,53**.

11. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the interconnect structure comprises copper.

12. The microsystem-on-a-chip of Claim 1, Okabe et al. show wherein the on or more via capture pads are sized to control the alignment tolerance of the thin upper chip.

Therefore, it would have been obvious to one of ordinary skill in the art to use the interconnect layer and the thin upper chip as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 2/6/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

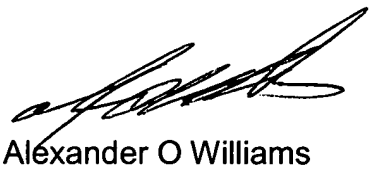
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,724,728,780,680,681,774,773,678, 679 174/52.4	11/5/05 4/26/06
Other Documentation: foreign patents and literature in 257/686,685,723,777,724,728,780,680,681,774,773,678, 679 174/52.4	11/5/05 4/26/06
Electronic data base(s): U.S. Patents	11/5/05 4/26/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/27/06